#### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Jan MULDER

Appl. No.: To Be Assigned (Cont. of Appl.

No. 10/158,774; Filed: May 31, 2002)

Filed: December 31, 2003

For: Analog To Digital Converter with Interpolation of Reference Ladder

Confirmation No.: To Be Assigned

Art Unit: To Be Assigned

Examiner: To Be Assigned

Atty. Docket: 1875.2810001/RES/GSB

#### Information Disclosure Statement

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicant has listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may

not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

- 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.
- 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final

Rejection, or Notice of Allowance, or an action that otherwise closes prosecution

	in the	application.
	☐ a.	Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of
	~	information contained in this Information Disclosure Statement was first
		cited in any communication from a foreign patent office in a counterpart
		foreign application not more than three months prior to the filing of this
		Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
	□ b.	Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of
		information in this Information Disclosure Statement was cited in a
		communication from a foreign patent office in a counterpart foreign
		application and, to my knowledge after making reasonable inquiry, was
		known to any individual designated in 37 C.F.R. § 1.56(c) more than
		three months prior to the filing of this Information Disclosure Statement.
		37 C.F.R. § 1.97(e)(2).
	□ c.	Attached is our PTO-2038 Credit Card Payment Form in the amount of
		\$ in payment of the fee under 37 C.F.R. § 1.17(p).
] 4.	Filing	under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being
	filed m	nore than three months after the U.S. filing date and after the mailing date
	of a Fi	nal Rejection or Notice of Allowance, but before payment of the Issue Fee.
	Enclos	ed find our PTO-2038 Credit Card Payment Form in the amount of
	\$	in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

- a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.
- 6. A concise explanation of the relevance of the non-English language document(s) appears below:
- 7. Copies of the documents are submitted herewith.

31, 2002, Application No. 10/153,709, filed May 24, 2002, Application No. 10/158,193, filed May 31, 2002, Application No. 10/158,595, filed May 31, 2002, and Application No. 10/158,773, filed May 31, 2002, which are relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO 1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

George S. Bardmesser Attorney for Applicant Registration No. 44,020

Date: \_\_\_\_December 31, 2003

1100 New York Avenue, N.W. Washington, D.C. 20005-3934 (202) 371-2600

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	AB1	6,62	28,224 B1	09/2003	Mulder et al.			
	AC1	6,51	8,898 B1	02/2003	Choksi			
	AD1	6,34	16,902 B1	02/2002	Venes et al.			
	AE1	6,48	39,913	12/2002	Hansen et al.			
	AF1	6,16	69,502	01/2001	Johnson et al.			-
	AG1		9,745 B1	07/2001	Chan			
	AH1	5,86	57,116	02/1999	Nakamura et al.			
	Al1 5,97		73,632	10/1999	Tai			
			4,943	09/1996	Moreland			
	AK1	5,42	2,642	06/1995	Chung et al.			
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	AR	1	Differential February 5	Architecture, , 2002, 3 pag	" IEEE International Solid-S es.	tate Circui	its Conference 2	002, IEEE,
Sushihara et al., "A 7b 450Msample/s 50mW CMOS ADC in 0.3 mm²," IEEE Solid-State Circuits Conference 2002, IEEE, February 5, 2002, 3 pages.  AS 1							nternational	
	AT	1	Dingwall ei State Circu	<i>t al.,</i> "An 8-M⊦ <i>iits</i> , Vol. SC-2	dz CMOS Subranging 8-Bit / 0, No. 6, December 1985, p	A/D Conve	erter," <i>IEEE Joui</i> 8-1143.	rnal of Solid-
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## FORM PTO-1449

**INFORMATION DISCLOSURE STATEMENT** 

ATTY. DOCKET NO. 1875.2810001/RES/GSB APPLICATION NO.
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FIRST NAMED INVENTOR

Jan MULDER FILING DATE

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INITIAL	AA2	NUM 5,471		DATE	NAME Wingender <i>et al</i> .	CLASS	SUB-CLASS	FILING DATE	
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	AC2	5,191	,336	03/1993	Stephenson				
	AD2	5,118	3,971	06/1992	Schenck				
	AE2	5,157	',397	10/1992	Vernon				
	AF2	5,006	,727	04/1991	Ragosch et al.				
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-	AH2	3,846,712		11/1974	Kiko				
	Al2	3,697	,978	10/1972	Prill				
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	AR	2	Abo, A.M. a	and Gray, P.R., "A nal of Solid-State	A 1.5-V, 10-bit, 14.3-MS/s CMC Circuits, Vol. 34, No. 5, May 19	)S Pipeline A 199, pages 59	ınalog-to-Digita 99-606.	I Converter,"	
	AS	2	Brandt, B.P. and Lutsky, J., "A 75-mW, 10-b, 20-MSPS CMOS Subranging ADC with 9.5 Effective Bits at Nyquist," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pages 1788-1795.						
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EXAMINER						DATE	CONSIDERED		

**EXAMINER**: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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	AR	<u>3</u>	Cho, T.B. a	OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Cho, T.B. and Gray, P.R., "A 10b, 20 Msample/s, 35 mW Pipeline A/D Converter," IEEE Jou Solid-State Circuits, IEEE, Vol. 30, No. 3, March 1995, pages 166-172.						
	Choe, MJ. et al., "A 13-b 40-Msample/s CMOS Pipelined Folding ADC with Background Offset Trimming," IEEE Journal of Solid-State Circuits, IEEE, Vol. 35, No. 12, December 2000, pages 1781-1790.							nd Offset ), pages 1781-		
	АТ	<u>3</u>	Choi, M. ar State Circu	nd Abidi, A., "A 6 iits," IEEE, Vol. 3	6-b 1.3-Gsample/s A/D Con 36, No. 12, December 2001	verter in 0.35-µm I, pages 1847-185	CMOS," IEEE .	Journal of Solid-		
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# FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO. 1875.2810001/RES/GSB APPLICATION NO.
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Page 4 of 11

FIRST NAMED INVENTOR Jan MULDER

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			Journal of	anu Sneanan, Solid-State Ci	rcuits, IEEE, Vol. 33, No.	12 December 1008	interpolating At	JC," IEEE
			Journal of	Cond-Glate Ch	realis, ILLL, Vol. 33, NO.	12, December 1990,	pages 1932-19	oo.
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			Geelen, G	6., "A 6b 1.1Gsa	ample/s CMOS A/D Conv	erter," IEEE Internation	onal Solid-State	Circuits
			Conference	ce, IEEE, Febru	uary 6, 2001, pages 128-1	129 and 438.		
	AS	4	ł					
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			Hoogzaad	I, G. and Roove	ers, R., "A 65-mW, 10-bit,	40-Msample/s BiCM	OS Nyquist AD	C in 0.8 mm <sup>2</sup> ,
			IEEE Jour	nal of Solid-Sta	ate Circuits, IEEE, Vol. 34	I, No. 12, December 1	999, pages 179	96-1802.
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		FORM	PTO-1449		FIRST NAMED INVI	1875.2810001/RES/GSB  FIRST NAMED INVENTOR Jan MULDER						
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	AR	<u>5</u>	Hosotani, Journal of	S. et al., "An 8- f Solid-State Cir	bit 20-MS/s CMOS A/D ( cuits, IEEE, Vol. 25, No.	Converter with 50-m' 1, February 1990, p	W Power Consu pages 167-172.	mption," <i>IEEE</i>				
	AS	<u>5</u>	Ingino, J. Journal of	and Wooley, B. f Solid-State Circ	, "A Continuously Calibra cuits, IEEE, Vol. 33, No.	ated 12-b, 10-MS/s, 3 12, December 1998	3.3-V A/D Conve , pages 1920-19	rter," <i>IEEE</i> 31.				
	АТ	<u>5</u>	Ito, M. et a	Ito, M. et al., "A 10 bit 20 MS/s 3 V Supply CMOS A/D Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 29, No. 12, December 1994, pages 1531-1536.								
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ATTY. DOCKET NO.	APPLICATION NO.	
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FIRST NAMED INVENTOR		
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# FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT

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	Kattman, K. and Barrow, J., "A Technique for Reducing Differential Non-Linearity Errors in Flash Converters, " <i>IEEE International Solid-State Conference</i> , IEEE, 1991, pages 170-171.  AR 6							
	AS	<u>6</u>	Kusumoto, I Solid-State	K. et al., "A 10-t Circuits, IEEE,"	o 20-MHz 30-mW Pipeline Vol. 28, No. 12, Decembe	ed Interpolating CMi er 1993, pages 1200	OS ADC," <i>IEEE</i> )-1206.	Journal of
	AT	<u>6</u>	Lewis, S. et Circuits, IEE	al., "A 10-b 20- EE, Vol. 27, No.	Msample/s Analog-to-Dig 3, March 1992, pages 35	ital Converter," <i>IEE</i> 1-358.	E Journal of So	lid-State
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	AR	<u>7</u>	Mehr, I. A Solid-Sta	and Singer, L., "A te Circuits, IEEE K. et al., "Efficier	nt 6-Bit A/D Converter Us 34, No. 8, August 1999, p	mple/s Nyquist-Ra 000, pages 318-3 ing a 1-Bit Folding	te CMOS ADC," II 25. g Front End," IEEE		
			µm Digita	K. et al., "A Dual I CMOS Process ges 1760-1768.	-Mode 700-Msamples/s 6 ," IEEE Journal of Solid-	6-bit 200-Msample State Circuits, IEE	es/s 7-bit A/D Con EE, Vol. 35, No. 12	verter in a 0.25- 2, December	

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	AR	<u>8</u>	IEEE Jour	and veries, A.,	ate Circuits, IEE	E, Vol. 30, No	o. 12, Decembe	d Interpolating A r 1995, pages 13	D Converter," 302-1308.
	AS	8	Pan, H. et Journal of	al., "A 3.3-V 12 Solid-State Cir	2-b 50-MS/s A/l cuits, IEEE, Vo	Converter ir I. 35, No. 12,	n 0.6µm CMOS December 2000	with over 80-dB ), pages 1769-17	SFDR," <i>IEEE</i> 780.
	АТ	8	Song, W Circuits, I	C. <i>et al.</i> , "A 10- EEE, Vol. 30, N	b 20-Msample/ o. 5, May 1995	s Low-Power , pages 514-5	CMOS ADC," <i>I</i> . 21.	EEE Journal of S	Solid-State
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			Taft, R. a	nd Tursi, M., "A	100-MS/s 8-b CMOS Subrang Down to 2.2 V," IEEE Journal of	ging ADC with	Sustained Param	netric
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			IEEE Jou	mal of Solid-Sta	te Circuits, IEEE, Vol. 34, No.	. 12, Decembe	er 1999, pages 18	03-1811.
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	AR	<u>11</u>	OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Yotsuyanagi, M. et al., "A 2 V, 10 b, 20 Msample/s, Mixed-Mode Subranging CMOS A/D Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 30, No. 12, December 1995, pages 1533-1537.								
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